Load-transient-response testing for voltage regulators

Semiconductor memory, card readers, microprocessors, disk drives, piezoelectric devices, and digital systems create transient loads that voltage regulators must service. Ideally, regulator output would be invariant during a load transient. In practice, however, some variation occurs, and this variation becomes problematic if a system exceeds its allowable operating-voltage tolerances. This problem mandates testing the regulator and its associated support components to verify desired performance under transient-loading conditions. You can use various methods to generate transient loads and allow observation of regulator response.

**Figure 1** shows a conceptual load-transient generator. The regulator under test drives dc and switched resistive loads, which may be manually variable. The device monitors its switched current and output voltage, permitting comparison of the output voltage and the load current under static and dynamic conditions. The switched current is either on or off; there is no electronically controllable linear region.

**Figure 2** shows a practical implementation of the load-transient generator. Capacitors augment the voltage regulator under test; these capacitors provide an energy reservoir, similar to a mechanical flywheel, to aid transient response. The size, dielectric, and location of these capacitors, particularly $C_{OUT}$, have a pronounced effect on transient response and overall regulator stability ([references 1 and 2]). The input pulse triggers the LTC1693 FET driver to switch $Q_1$, generating a transient-load current from the regulator. A wideband oscilloscope monitors the instantaneous load voltage and, through a “clip-on” wideband-probe, current (see sidebar “Probing considerations for load-transient-response measurements”). **Figure 3** provides an evaluation of the circuit’s load-transient-generating capabilities by substituting a low-impedance power source for the regulator. The combination of a high-capacity power supply, low-impedance connections, and generous bypassing maintains low impedance across frequency. **Figure 4** shows the circuit in **Figure 3**’s response to the LTC1693-1 FET driver (Trace A) by cleanly switching 1A in 15 nsec (Trace B). Such speed is useful for simulating many loads but has restricted versatility. Although fast, the circuit cannot emulate loads between the minimum and the maximum currents.

**CLOSED-LOOP TESTERS**

**Figure 5**’s conceptual closed-loop load-transient generator linearly controls $Q_1$’s gate voltage to set instantaneous transient current at any desired point, allowing simulation of nearly any load profile. Feedback from $Q_1$’s source to the $A_1$ control amplifier closes a loop around $Q_1$, stabilizing its operating point. $Q_1$’s current assumes a value that depends on the control-input voltage and the current-sense resistor over a wide bandwidth. Once $A_1$ biases to $Q_1$’s
conductance threshold, small variations in $A_1$'s output result in large current changes in $Q_1$'s channel. As such, $A_1$ need not output large excursions; its small signal bandwidth, rather than its slew rate, is the fundamental speed limitation. Within this restriction, $Q_1$'s current waveform is the same shape as $A_1$'s control-input voltage, allowing linear control of load current. This versatile capability permits a variety of simulated loads.

**FET-BASED CIRCUIT**

Figure 6 shows a practical incarnation of a FET-based closed-loop load-transient generator, including dc-bias and waveform inputs. $A_1$ must drive $Q_1$'s high-capacitance gate at high frequency, necessitating high peak $A_1$ output currents and attention to feedback-loop compensation. $A_1$, a 60-MHz current-feedback amplifier, has an output-current capacity exceeding 1A. Maintaining stability and waveform fidelity at high frequency while driving $Q_1$'s gate capacitance necessitates settable gate-drive-peaking components, a damper network, feedback trimming, and loop-peaking adjustments. You make the required dc trim first. Without applying an input, trim the 1-mV adjust for 1 mV dc at $Q_1$'s source. You make the ac trims using Figure 7's arrangement. Similar to the circuit in Figure 3, this "brick-wall"-regulated source provides minimal ripple and sag when the load-transient generator step-loads it. A pply the inputs as the figure shows and trim the gate drive, feedback, and loop-peaking adjustments for the cleanest square-cornered response on the oscilloscope's current-probe-equipped channel.

**BIPOLAR TRANSISTORS**

The circuit in Figure 8 considerably simplifies the previous circuit's loop dynamics and eliminates all ac trims. The major trade-off is a halving of speed. The circuit is similar to the one in Figure 6, except that $Q_1$ is a bipolar transistor. The bipolar's greatly reduced input capacitance allows $A_1$ to drive a more benign load. This approach permits you to use an amplifier with lower output current and eliminates the dynamic trims necessary to accommodate Figure 6's FET-gate capacitance. The sole trim is the 1-mV adjustment, which you accomplish as described. You can eliminate this trim at the cost of circuit complexity (see sidebar "A trimless, closed-loop-transient-load tester"). A side from the twofold speed decrease, the bipolar transistor also introduces a 1% output-current error due to its base current. You add $Q_2$ to prevent excessive $Q_1$ base current when the regulator supply is absent. The diode prevents reverse-base bias under any circumstances.

**CLOSED-LOOP-CIRCUIT PERFORMANCE**

Figures 9 and 10 show the two wideband circuits' operation. The FET-based circuit (Figure 9) requires only a 50-mV $A_1$ swing (Trace A) to enforce Trace B's flat-topped current pulse with 50-nsec edges through $Q_1$. Figure 10 details the bipolar-transistor-based circuit's performance. Trace A, taken at $Q_1$'s regulator-input supply

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**Figure 3** Substituting a well-bypassed, low-impedance power supply for the regulator lets you determine the load tester's response time.

**Figure 4** Figure 2's circuit responds to the FET driver's output (Trace A), switching a 1A load (Trace B) in 15 nsec.

**Figure 5** In this conceptual closed-loop-load tester, $A_1$ controls $Q_1$'s source voltage, setting the regulator's output current. $Q_1$'s drain-current waveshape is identical to $A_1$'s output, allowing linear control of the load current. The voltage and current monitors match those in Figure 1.
base, rises less than 100 mV, causing Trace B’s clean, 1A current conduction through Q1. This circuit’s 100-nsec edges, about two times slower than the more complex FET-based version, are still fast enough for most practical transient-load testing.

LOAD-TRANSIENT TESTING

These circuits permit rapid and thorough voltage-regulator load-transient testing. Figure 11 uses Figure 6’s circuit to evaluate an LT1963A linear regulator. Figure 12 shows regulator response (Trace B) to Trace A’s asymmetrically edged input pulse. The ramped leading edge, within the LT1963A’s bandwidth, results in Trace B’s smooth 10-mV p-p excursion. The fast trailing edge, well outside the LT1963A’s passband,
Figure 9 Figure 6’s closed-loop-load-tester step response is quick and clean, showing 50-nsec edges and a flat top. (Q1’s current is Trace B.) A1’s output (Trace A) swings only 50 mV, allowing wideband operation. Trace B’s presentation is slightly delayed due to voltage and current-probe time skew.

Figure 10 Figure 8’s bipolar-output-load-tester response is two times slower than the FET version, but the circuit is simpler and eliminates compensation trims. Trace A is A1’s output, and Trace B is Q1’s collector current.

Figure 11 This closed-loop-load tester with an LT1963A regulator provides load testing for a variety of current and load waveshapes.

Figure 12 The circuit in Figure 11 responds (Trace B) to an asymmetrically edged pulse input (Trace A). A ramped leading edge within the LT1963A’s bandwidth results in Trace B’s smooth, 10-mV-p-p excursion. A fast trailing edge outside the LT1963A’s bandwidth causes Trace B’s abrupt 75-mV-p-p disruption. The photo intensifies the trace’s latter portion for clarity.

Figure 13 A 500-mA-p-p, 500-kHz noise load (Trace A) within the regulator’s bandpass produces only 6-mV artifacts at Trace B’s regulator output.
causes Trace B’s abrupt disruption. C\textsubscript{OUT} supplies too little current to maintain output level, and a 75-mV-p-p spike results before the regulator resumes control. In Figure 13, a 500-mA p-p, 500-kHz noise load, emulating a multitude of incoherent loads, feeds the regulator in Trace A. This frequency is within the regulator’s bandwidth, and only 6 mV p-p of disturbance appears in Trace B, the regulator output. Figure 14 maintains the same conditions, except that noise bandwidth increases to 5 MHz. This increase exceeds regulation bandwidth, resulting in more than 50-mV p-p error, an eightfold increase.
CAPACITOR’S ROLE IN REGULATOR RESPONSE

The regulator employs capacitors at its input (C_in) and output (C_out) to augment its high-frequency response. You should carefully consider the capacitor’s dielectric, value, and location because they greatly influence regulator characteristics (references 1, 2, and 3). C_out dominates the regulator’s dynamic response; C_in is much less critical, as long as it does not discharge below the regulator’s dropout point. Figure 16 shows a typical regulator circuit and emphasizes C_out and its parasitics. Parasitic inductance and resistance limit capacitor effectiveness at frequency. The capacitor’s dielectric and value significantly influence load-step response. A “hidden” parasitic, impedance buildup in regulator-output-trace runs, also influences regulation characteristics, although you can minimize the parasitic’s effects by remote sensing and distributed capacitive bypassing.

Figure 17 shows Figure 16’s circuit responding (Trace B) to a 0.5A load step biased on 0.1A dc (Trace A) with C_in/C_out = 10 μF. The circuit employs low-loss capacitors, resulting in Trace B’s well-controlled output. Figure 18 greatly expands the horizontal time scale to investigate high-frequency behavior. Regulator-output deviation (Trace B) is smooth with no abrupt discontinuities. Figure 19 runs the same test as Figure 17 using an output capacitor claimed as “equivalent” to the one that Figure 17 employs. At 10 μsec/division, the scope photos seem similar, but Figure 20 indicates problems. This photo, taken at the same higher sweep speed as the one in Figure 18, reveals the “equivalent” capacitor to have twice as much amplitude error, higher frequency content, and higher resonances than the one in Figure 18. (Always specify components according to observed performance, rather than salesmen’s claims.) Figure 21 substitutes a lossy 10-μF unit for C_out. This capacitor allows a 400-mV excursion (note Trace B’s vertical-scale change), greater than four times Figure 18’s amount. Conversely, Figure 22 increases C_out to a low-loss, 33-μF type, decreasing Trace B’s output-response transient by 40% versus Figure 18. Figure 23’s further increase, to a low-loss, 330-μF capacitor, keeps transients inside 20 mV: four times lower than Figure 18’s 10-μF value.

The lesson is clear: Capacitor value and dielectric quality have a pronounced effect on transient-load response. Try before specifying!

RISE TIME VERSUS REGULATOR RESPONSE

The closed-loop-load-transient generator also allows investigating load-transient rise time on regulation at high speed. Figure 24 shows Figure 16’s circuit (C_in/C_out = 10 μF), respond-
PROBING CONSIDERATIONS FOR LOAD-TRANSIENT-RESPONSE MEASUREMENTS

Signals of interest in load-transient-response studies occur within a bandwidth of approximately 25 MHz and a rise time of 14 nsec. This modest speed range eases probing techniques, but high-fidelity measurement requires some care. You measure load current with a dc-stabilized, Hall-effect, clip-on current probe such as the Tektronix (www.tektronix.com) P-6042 or A6302/AM503. The conductor loop in the probe jaws should encompass the smallest possible area to minimize introduced parasitic inductance, which can degrade measurement. At higher speeds, grounding the probe case may slightly decrease measurement aberrations, but this effect is usually small.

You perform voltage measurement, typically ac-coupled and ranging from 10 to 250 mV, using the arrangement in Figure A. This arrangement feeds the measured voltage to a BNC 50Ω, back-terminated cable, which drives the oscilloscope through a dc-blocking capacitor and a 50Ω termination. The back termination is strict practice, enforcing a true 50Ω signal path. You can eliminate the unit’s 6-dB attenuation if it presents problems with only minor signal degradation in the 25-MHz measurement passband. The termination at the oscilloscope end is not negotiable. Figure B shows a typical observed load transient with no back termination but 50Ω at the oscilloscope. The presentation is clean and well-defined. Figure C removes the cable’s 50Ω termination, causing a distorted leading edge, ill-defined peaking, and pronounced postevent ringing. Even at relatively modest frequencies, the cable displays unterminated-transmission-line characteristics, resulting in signal distortion.

In theory, a 1X scope probe using a probe-tip coaxial connection could replace the described circuit, but such probes usually have bandwidth limitations of 10 to 20 MHz. Conversely, a 10X probe is wideband, but the oscilloscope’s vertical sensitivity must accommodate the introduced attenuation.

Figure A A coaxial-load transient voltage-measurement path promotes observed signal fidelity. You can remove the 50Ω back termination with minimal impact on the 25-MHz signal path’s integrity.

Figure B Observing a typical high-speed transient through Figure A’s measurement path presents a clean and well-defined signal.

Figure C Measuring Figure B’s transient without the 50Ω oscilloscope’s termination shows results in waveform distortion and postevent ringing.
ing to a 0.5A, 100-nsec rise-time step on a 0.1A dc load (Trace A). Response decay (Trace B) peaks at 75 mV with some following aberrations. Decreasing Trace A’s load-step rise time (Figure 25) almost doubles Trace B’s response error, with attendant enlarged following aberrations. This scenario indicates increased regulator error at higher frequency.

All regulators present increasing error with frequency—some more than others. A slow load transient can unfairly make a poor

Figure 24 The regulator’s output response (Trace B) to a 100-nsec rise-time current step (Trace A) for C\textsubscript{OUT} is 10 \(\mu\)F. The response decay peaks at 75 mV.

Figure 25 Faster rise-time current step (Trace A) increases response-decay peak (Trace B) to 140 mV, indicating increased regulation loss versus frequency.

Figure 26 The P30 embedded-memory voltage regulator must maintain a ±0.1V error band. Control-line movement causes 50-mA load steps, necessitating attention to C\textsubscript{OUT} selection.

Figure 27 A 50-mA load step (Trace A) results in 30-mV regulator-response peaks, two times better than error-budget requirements. C\textsubscript{OUT} is a low-loss, 1-\(\mu\)F capacitor.

Figure 28 Increasing the value of C\textsubscript{OUT} to 10 \(\mu\)F decreases regulator-output peaks to 12 mV, almost six times better than required.

Figure 29 A low-grade, 10-\(\mu\)F C\textsubscript{OUT} causes 100-mV regulator-output peaks (Trace B), violating the P30 regulator’s memory limits. The scope photo intensifies the trace’s latter portion for clarity.

<table>
<thead>
<tr>
<th><strong>TABLE 1</strong> Intel P30 Embedded-Memory Voltage-Regulator Error Budget</th>
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<tbody>
<tr>
<td><strong>Parameter</strong></td>
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<tr>
<td>Intel-specified supply limits</td>
</tr>
<tr>
<td>LTC1844 regulator initial accuracy</td>
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<tr>
<td>Dynamic-error allowance</td>
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A TRIMLESS, CLOSED-LOOP-TRANSIENT-LOAD TESTER

Eliminating a FET-based design’s ac trims is an attractive option; however, eliminating the dc trim is also important. The circuit in Figure A trades circuit complexity to achieve this goal. The circuit includes two amplifiers, A₁ and A₂.

Figure A. A₂’s feedback controls A₁’s dc errors, eliminating trim. Filtering restricts A₁’s response to dc and low frequency.

A₁ replaces the dc trim by measuring the circuit’s dc input and comparing it with Q₁’s emitter dc level and controlling A₁’s positive input to stabilize the circuit. The system filters high-frequency signals at A₁’s inputs, and these signals do not corrupt A₁’s stabilizing action. A useful way to consider circuit operation is that A₁ balances its inputs and, hence, the circuit’s input and output, regardless of A₁’s dc-input errors. You can set the dc-current bias to any desired point by directing a variable reference source to A₁’s positive input. The arrangement of the network’s resistors yields a minimum load current of 10 mA, avoiding loop disruption for currents near zero.

regulator look good. Transient-load testing that does not indicate some response outside regulator bandwidth is suspect.

The Intel [www.intel.com] embedded-memory voltage regulator furnishes a good, practical example of the importance of voltage-regulator-load-step performance. The memory requires a 1.8V supply, typically regulated down from 3V. Although current requirements are relatively modest, supply tolerances are tight. Table 1 shows only 0.1V allowable excursion from 1.8V, including all dc and dynamic errors. The LT1844-1.8 regulator has a 1.75% initial tolerance at 31.5 mV, leaving only a 68.5-mV dynamic-error allowance. Figure 26 shows the test circuit. Memory-control-line movement causes 50-mA load transients, necessitating attention to capacitor selection. (The LT1844-1.8’s noise-bypass pin works with an optional external capacitor to achieve low output noise. This application, however, does not require it, and remains unconnected.) If the regulator is close to the power source, Cᵢᵢ is optional. If not, use a high-grade, 1-μF capacitor for Cᵢᵢ. Cᵦᵦᵢᵢ is a low-loss, 1-μF type. In all other respects, the circuit appears deceptively routine. A load-transient generator provides Figure 27’s output-load test step (Trace A). This test uses Figure B’s circuit and changes Q₁’s emitter-current shunt to 1Ω. Trace B’s regulator response shows just 30-mV peaks, more than two times better than necessary. Increasing Cᵦᵦᵢᵢ to 10 μF (Figure 28) reduces peak output error to 12 mV, almost six times better than specification. However, a low-grade 10-μF—or 1-μF, for that matter—capacitor produces Figure 29’s unwelcome surprise. Severe peaking error on both edges occurs with 100-mV observable on the negative-going edge. (The photograph shows an intensified version of Trace B’s latter portion to aid clarity.) This figure is well outside the error budget and would cause unreliable memory operation (references 4, 5, and 6). EDN

REFERENCES
3. LT1584/LT1585/LT1587 Fast Response Regulators Data Sheet, Linear Technology Corp.
4. LT1963A Regulator Data Sheet, Linear Technology Corp.

AUTHOR BIOGRAPHY
Long-time EDN contributor Jim Williams, staff scienti at Linear Technology Corp (M I li tias, C A.), has more than 20 years’ experience in analog-circuit and instrumentation design.