Offline power supplies that drive loads of 200W and more require inrush-current limiters. Unrestricted inrush currents can reach hundreds of amperes, which may damage the line rectifier, open the fuse and input-filter inductors, and damage the PFC (power-factor-correction) filter capacitors. A simple method of limiting the inrush current uses an NTC (negative-thermal-coefficient) thermistor that connects in series with the supply line. When cold, the thermistor presents a high resistance, but its resistance decreases significantly as its temperature increases, limiting the inrush current by virtue of its thermal inertia and inability to quickly decrease its resistance.

However, an NTC thermistor also presents some resistance to the power supply's normal operating current. To keep the thermistor's normal resistance low, it should operate at a sustained and relatively high temperature, but this scenario may impair the power supply's temperature profile and raise the temperature in an enclosure in which power dissipation is already substantial.

This Design Idea offers an alternative circuit that effectively limits inrush current and does not add an extra source of heat to the power-supply package. Without increasing power losses during normal operation, a switchable series resistor in the power supply's dc section can efficiently limit inrush current until the PFC-rail electrolytic capacitors acquire a full charge. Then, an electromechanical or optically isolated semiconductor relay short-circuits the resistor.

However, determining whether the PFC capacitors are fully charged presents a problem. Universal power-supply designs operate over a range of ac-input voltages, and determining the voltage that indicates a full charge can thus prove elusive. In addition, the inrush-current limiter should delay operation of any internal auxiliary power supplies and other power-consuming circuits to allow the PFC-rail capacitors to charge to their full predetermined extent.

The easiest method of solving these problems is to use a simple and effective inrush-current limiter, which stops surges. Figure 1 shows such a circuit, which features an electromechanical relay, $S_1$, and a current-limiting resistor, $R_1$. (Unless otherwise mentioned, all resistors in the schematic are rated for 0.125W.)

**Figure 1** This inrush-current-limiter circuit features an electromechanical relay, $S_1$, and a current-limiting resistor, $R_1$. (Unless otherwise mentioned, all resistors in the schematic are rated for 0.125W.)
problems uses a circuit that measures the inrush current itself and not the voltage across the PFC capacitors. It determines the end of the inrush process by monitoring extinction of the inrush current’s amplitude. Upon reaching a preset threshold, the circuit commands the start-up of auxiliary power supplies and other circuits. Monitoring the inrush current allows effective control of the power supply’s starting point and renders the start-up threshold independent of the input-line voltage.

Figure 1 shows a practical version of a PFC circuit, which employs a switched-resistor inrush-current limiter. The inrush-current-sensing subcircuit comprises a wirewound resistor, R1, and a parallel depletion-mode MOSFET, Q1, which connects to resistor R2 as a current source that drives resistors R3 and R4. Over a wide range of the voltage drop across R1, from a few hundred volts to a few volts, this circuit generates a small constant current that suppresses operation of the auxiliary power supply and prevents interference with the inrush-current-limiting process.

When the inrush current decreases sufficiently, the voltage drop across R1 becomes insufficient to keep Q1 in operation as a current source. Q1’s current extinguishes, allowing the auxiliary power supply to turn on and start the power supply, by activating relay S1, whose contacts short-circuit R1. R2’s value determines the current necessary to hold the auxiliary power supply in a disabled mode, allowing PFC-rail capacitor C1 to charge fully.

A 12V electromechanical relay, such as Omron’s (www.omron.com) G2RL-1, provides low-resistance contacts to bypass R1 (Reference 1). As an alternative, an optically isolated solid-state relay, such as the Carlo Gavazzi (www.gavazzionline.com) RP1A48D5, with a MOSFET or an SCR (silicon-controlled-rectifier) output device can replace S1, provided that the voltage drop across the output device introduces no substantial power loss (Reference 2).

Figure 2 depicts the charging process’s waveform as the voltage drop across R1. The exponential envelope and its subcycles represent components of the inrush process; R1 and C2 filter out the subcycles and produce a decreasing exponential voltage waveform across R4, holding Q2 on for the duration of the inrush process. Q1 suppresses the auxiliary power supply’s operation by pulling its disable input low. At a few volts across R1, Q1 stops generating constant current and shuts down Q2 to enable the auxiliary power supply. Thus, the entire power supply waits until the inrush current attains a safe value that R1 sets. The power supply starts immediately after relay S1 trips and shorts out inrush resistor R1. The remainder of Figure 1 comprises a conventional PFC but may also represent a part of any other power-supply configuration.

Trace 1 in Figure 3 depicts the start-up of a 2.4-kW power supply with the inrush-current limiter and a slow-start
Inverting sample-and-hold amplifier requires no external resistors

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Many applications require a sampling circuit whose output is inverted with regard to the respective sample of an input signal. A simple approach is a cascade of a common noninverting sample-and-hold amplifier and an inverting amplifier. A classic inverting amplifier is an op amp with voltage feedback from two resistors. The values of these resistors, which are usually equal, should be high enough to decrease the total power loss...
of \( P = 2V^2/R_1 \), which is proportional to the square of the output voltage. The values of these resistors should be as low as possible to preserve the bandwidth of the op amp.

Any parasitic capacitance \( C_2 \) in the following equation parallel to feedback resistor \( R_1 \) forms a pole in the transfer function of the inverter. This pole results in an additional breakdown of the gain-frequency characteristic of the inverting amplifier, with the value of breakdown frequency of \( f_b = (1/2\pi)(1/R C_1) \). To retain the widest possible bandwidth, \( f_c > f_p \), where \( f_c \) is the transition frequency of the op amp—in other words, the frequency at which the open-loop gain of the op amp drops to unity.

The Analog Devices’ (www.analog.com) AD8592 dual op amps, which have a high-quality shutdown function, allow you to use a different approach (Reference 1). The inverting sample-and-hold circuit in Figure 1 uses no external resistors. Thus, no power dissipates at external passive devices in the hold state of the circuit. All op amps act as voltage followers. In the hold state, followers \( B_2 \) and \( A_2 \) are enabled; thus, the \( B \) lead of the \( C_2 \) capacitor, Pin 1 of IC2, is grounded through the output of the \( A_2 \) follower. This scenario causes a negative voltage of \( -V_s \) to appear at the input of the \( B_2 \) voltage follower, which in turn charges the \( C_2 \) capacitor to the voltage of \( -V_s \) at the beginning of the sampling command. Voltage follower \( A_1 \) serves as an impedance converter.

The AD8592’s data sheet does not directly specify the leakage current at the output of the voltage follower; however, you can estimate it as being lower than 10 pA. Capacitors \( C_1 \) and \( C_2 \) thus can have unusually low values. On the other hand, the op amps’ high output current of 250 mA contributes further to the fast charging of capacitors \( C_1 \) and \( C_2 \).

The \( B_2 \) voltage follower serves as a delay line, which, in conjunction with one AND gate and one NOR gate, generates two semicomplementary logic-control signals (Figure 2). Both of these signals, \( Q_S \) and \( \overline{Q}_S \), are thus kept at an inactive low level for a sufficiently long time, before moving to an active high level, providing a break-before-make operation. The input voltage gets tracked at the \( C_1 \) capacitor with \( \overline{Q}_S \) high, and the last value of this voltage, at the high-to-low transition of \( Q_S \), is a sample. The sample, at the instant of the low-to-high transition of \( Q_S \), appears with a negative sign at capacitor \( C_2 \) and subsequently at the output.

REFERENCE


Single IC forms inexpensive inductance tester

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This Design Idea shows how to build a reliable, low-cost, and simple inductance tester. The basis for the tester is a Pierce buffered CMOS oscillator (Figure 1). Instead of using the usual quartz crystal, you connect the inductor under test. This oscillator uses a single CMOS inverter biased through resistor \( R_1 \) in its linear region to form a high-gain inverting amplifier. Because of its high gain, the inverter dissipates lower power than an unbuffered gate; even a small signal drives the output high and low. The \( LC\pi \) network forms a parallel resonator that ideally resonates at the frequency \( f_0 = 1/2\pi\sqrt{L_3/C_3} \), which corresponds to a period, \( T_{30} \), of \( 2\pi\sqrt{L_3/C_3} \), where \( C_3 = \frac{1}{2}C_1 || C_2 = 50 \text{ nF} \). So, you can calculate the inductance, \( L_3 \), by measuring the resonant frequency, \( f_0 \), or the period, \( T_{30} \). At the resonant frequency, the \( LC\pi \) network provides a 180° phase shift from input to output. To oscillate, the phase shift at frequency \( f_1 \), around the oscillator loop must be 360°, and the gain of the oscillator loop must be greater than one. Inverter IC1A provides an addi-
tional 180° phase shift from input to output and a high gain to compensate for the attenuation of the network.

Resistor \( R_1 \) is not critical, and its value can be 1 to 10 M\( \Omega \). Resistor \( R_2 \) isolates the output of gate IC\(_{1A}\) from the LC\( \pi \) network so that you can obtain a nearly clean square wave from the output of the gate itself. In addition, \( R_2 \) improves frequency stability because it increases the slope of phase shift around the resonant frequency. For best performance, use film capacitors with low self-inductance, such as the MKP1837 polypropylene-film capacitors series with 1% tolerance from Vishay (www.vishay.com). You can also use other film capacitors with standard tolerance provided that you select the value with a precision capacitance tester for best accuracy. The low supply current of the circuit allows you to use a battery as a power source.

**Figure 1** Replacing a Pierce oscillator’s crystal with an unknown inductance allows you to measure its value by observing the resulting oscillation’s frequency.